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Practical nanoscale field emission devices for integrated circuits

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Nanoscale field emission devices promise many advantages over traditional solid-state devices including fast switching speeds, extreme operating temperatures, and radiation hardness. Despite this, practical circuits have long been hampered by the extreme requirements of nanoscale field emitters. Devices have required vacuum packaging, or extremely sharp emission points that are difficult to reproduce, or cannot be integrated on a single wafer with independent gating. We demonstrate CMOS compatible, integratable two- and three-terminal devices operating at near atmospheric pressures with high single tip currents at low voltages that can be used as building blocks for future circuits. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4989677]

Cold-cathode field emission has been explored for decades, first as a possible replacement for cathode ray tube displays[1] and later for bright electron sources for X-ray spectroscopy.[2] More recently, researchers have begun to demonstrate the feasibility of field emission devices as circuit elements.[3] Field emission devices are promising candidates for future electronics for several reasons. The quantum mechanical nature of electron field emission, combined with ballistic transport through the vacuum, can produce devices with GHz operating frequencies when device dimensions are micron scale.[4] Reducing the vacuum gap dimensions to less than 100 nm could theoretically produce transistors that can be operated at frequencies of 100 GHz or more.[5] Solid-state transistors fail at high temperature when electrons in the p-doped regions are thermally excited to the same conduction electron concentration as in the n-doped regions. This effectively eliminates p-n junctions, limiting the maximum operating temperature for silicon MOSFETs to approximately 300 °C,[6] and silicon carbide (SiC) transistors to 600 °C.[7] Field emission devices can be operated at elevated temperatures because the device current remains exponentially dependent on the field until much higher temperatures where thermionic emission dominates. Recently, SiC nanoneedle field emitting arrays have been successfully operated at 500 °C.[8] Moreover, high radiation environments shorten the lifetime of solid-state transistors by damaging the crystal lattice of the semiconductor, decreasing minority carrier lifetimes and increasing the resistance.[9] Since carrier lifetimes are less critical for field emission operation, these devices have long been considered prime candidates for radiation-hard electronics.

Shrinking device dimensions below 200 nm allows field-emitting devices to operate at atmospheric pressure since the mean free path of electrons at these pressures exceeds this distance.[10,11] Field emitters can be made in SOI as shown by Han *et al.*[5] and gated by applying a potential to the handle, but this design makes implementing multi-transistor circuits on a wafer difficult. We demonstrate a paradigm for CMOS compatible, low voltage, robust devices, which are operational at atmospheric pressures and can be independently gated on a single integrated chip. We achieve the high fields necessary for field emission at low voltages by creating short emitter-collector gaps via electron beam lithography, as opposed to relying on atomic protrusions to create low voltage turn-ons as in the study by Pescini *et al.*[11] This strategy provides the reproducibility needed to make many robust devices on a single chip.

Cold field emission involves the tunneling of electrons from a conductor into the vacuum in the presence of an intense surface electric field. The applied electric field bends the vacuum level outside of the conductor, causing the energy of the vacuum state to drop to the energy of the conduction electrons in the metal. This allows the electrons to tunnel to free space. The phenomenon is governed by a Fowler-Nordheim type equation.[12] For emission from a non-flat metallic surface[11]

$$I = \lambda A a \frac{1}{\phi} E^2 \exp\left(\frac{-b\phi^{\frac{3}{2}}}{E}\right),$$

$$a \approx 1.54 * 10^{-6} \frac{Amps * eV}{V^2},$$

$$b \approx 6.83 * 10^{9} (eV)^{-3/2} \frac{V}{m},$$

where A is the field emission area, E = kV is the electric field at the point of emission for a voltage V, and λ is a factor that depends on the geometry of the emitter. The factor k is the static field enhancement and also depends on the device geometry. Designs including silicon oxide sharpening or atomic protrusions experience a higher field enhancement, which can partially compensate for larger emitter-collector gaps. To distinguish cold cathode field emission from other conduction mechanisms, current-voltage data are typically plotted in the so-called Fowler-Nordheim coordinates, where the x-axis is plotted in units of 1/V and the y-axis in units of $\log(I/V^2)$. True cold cathode field emission should be linear in these coordinates.[13]

To demonstrate our design paradigm, we first fabricate two-terminal devices. We begin with a silicon-on-insulator substrate (SOI, 220 nm Si/2000 nm SiO_2). The single-crystal silicon device layer is n-doped with phosphorus to a surface conductivity of approximately 5 kΩ using a Desert Silicon P-260 spin-on dopant. We then spin coat a layer of diluted Microchem poly(methyl methacrylate) (PMMA) A2 950 and pattern this resist with 100 keV electron beam lithography.

We deposit 12 nm of Al_2O_3 over the silicon layer by electron beam evaporation and perform liftoff. Using Al_2O_3 as a hardmask, the device and contact pads are etched into the silicon device layer. To etch the silicon layer, we use a mixed-mode Bosch etch consisting of SF6 as an etch gas and C_4F_8 as a passivation layer. Contact pads to each terminal are made by photolithography followed by a wet etch step in 5% tetramethylammonium hydroxide (TMAH) to remove the Al_2O_3 layer over the contacts, followed by gold contact metal deposition and liftoff.

Devices are pumped to a pressure of 10^{-5} Torr for several hours prior to testing to allow the desorption of water and other contaminants from the emitting surfaces. The devices are then measured in-situ using a custom-built probe station. A heated stage and attached thermocouple allows the temperature of the devices during testing to be varied from near room temperature to over 500 °C. To test the devices at different pressures, the chamber is backfilled with argon gas to a desired pressure.

Shown in the bottom inset of Fig. 1 is a scanning electron micrograph of a representative two-terminal field emission device. By designing the relative sharpness of each tip, we can create an asymmetric current-voltage characteristic, shown in the main body of Fig. 1. When biased to emit electrons from the sharp tip (shown in the red portion of the graph and hereafter referred to as the forward direction), emission occurs at a lower voltage. This is because the sharp tip experiences greater static field enhancement than the dull tip. This asymmetric behavior of lateral devices is important for replicating the rectification behavior of existing solid-state diodes.

The top inset in Fig. 1 shows the current-voltage characteristic of the same device in Fowler-Nordheim coordinates, ignoring currents below 30 nA. We see from the linear nature of the plot that the currents above 30 nA are due to Fowler-Nordheim emission. The instability observed in the forward direction at higher voltages is likely caused by changes in the emitter, probably as a result of current-induced heating. We

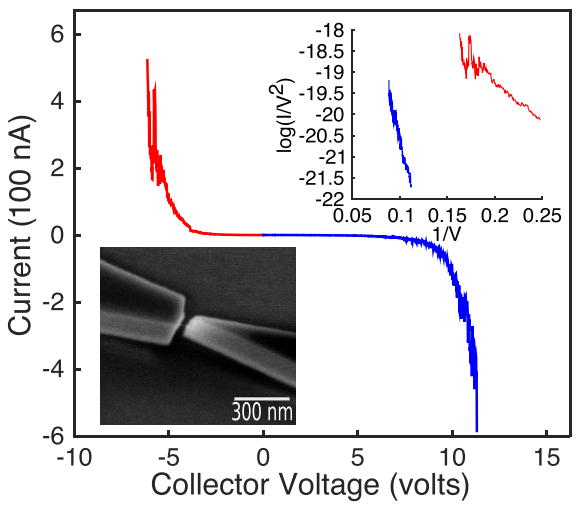


FIG. 1. Two-terminal IV characteristic. The red portion represents emission from the sharpened tip, and the blue portion represents emission from the blunt tip. A scanning electron micrograph of the device is shown in the bottom inset. The emitter-collector gap is 22 nm. The Fowler-Nordheim characteristic is plotted in the top inset for currents greater than 30 nA. The straight line nature of the characteristic indicates that the conduction mechanism is indeed Fowler-Nordheim.

also performed time series operations of the two-terminal device. Over the course of 1 hour while held at a constant potential, the emitter produced a constant current of 250 nA in the forward direction with fluctuations of approximately 40%. Single tip field emitter current instabilities are often attributed to field induced atomic motion at the tip.[14] Lower current fluctuations can be achieved by adding more field emission tips at the cost of increased device capacitance.[15]

We calculate the work function of the above device using a combination of measured current-voltage data and COMSOL simulations derived from SEMs of the specific device. We can fit the slope of the FN graph to obtain an experimental value for $\frac{-b\phi^{\frac{3}{2}}}{k}$. We obtain device dimensions from scanning electron micrographs of each specific device and build 2D COMSOL simulations to estimate the static field enhancement factor, k. From simulation, these values obtained are $k = 6.15 \times 10^7$ 1/m in the forward direction and $k = 3.68 \times 10^7$ 1/m in the reverse direction. From this, we obtain an estimated work function of 3.21 eV in the forward direction and 1.6 eV in the reverse direction. The accepted value for the work function of bulk silicon is 4.05 eV,[16] but strong phosphorus doping can produce work functions as low as 2eV,[17] and finally, the presence of adsorbed molecules at the emission site can change the work function even further.

Single tip field emission devices are particularly susceptible to surface contamination and tip destruction. Surface adsorbates can alter the local work function upon which the current exponentially depends.[18] Additionally, the emitted current can ionize atoms that can then collide with the tip, blunting or destroying the devices. By shrinking the emitter-collector gap, we reduce the need to have a sharp tip to produce low voltage emission. This minimizes the effect of surface changes, either by contamination or by ion impact. Additionally, by operating at potentials lower than 12 volts, emitted electrons do not have sufficient energy to ionize common gas species,[19] which further reduces tip degradation.

Following our work with two-terminal devices, we extended our geometry to produce an in-plane gated three-terminal device. This was done by combining the layered approach of Srisonphan *et al.*[20] with the design of our two-terminal devices as shown in the inset of Fig. 2. As with the diode case, the bottom layer consists of a doped silicon emitter and a collector. A high quality dielectric Al_2O_3 layer, deposited by atomic layer deposition (ALD), separates the silicon layer from a metallic gate layer. The application of a bias voltage to the gate layer modifies the field at the emitter tip, modulating the current between the emitter and the collector. By combining a high work function gate material with a high dielectric strength oxide, one can limit the leakage current either through field emission from the gate or from oxide leakage. For this study, chrome with a work function of 4.5 eV (Ref. 16) was used as the gate material to facilitate fabrication since it is compatible with later etching processes. A critical improvement in this design over the use of backplane gating is that these devices can be gated separately, a necessity for the integration of many devices on a single wafer.

To fabricate the gated field emission device, we begin with the same SOI substrate (220 nm/2000 nm) as was used for the two-terminal devices. The device layer is again doped with

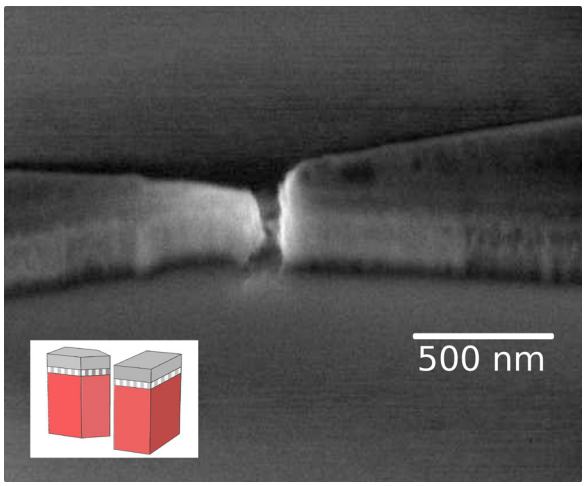
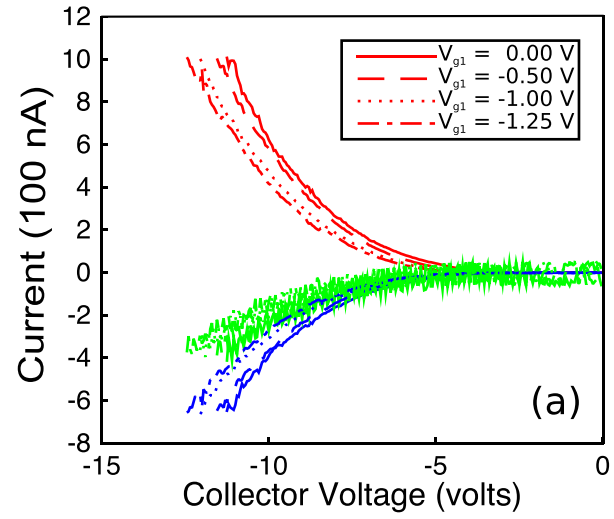


FIG. 2. Gated field emission device at 45° tilt. The emitter collector gap is 68 nm. The inset shows a diagram of the layered structure of the device. The red layer represents the doped silicon emitter and collector layer, the grey region the chromium gate layer, and the striped region the ALD alumina layer. The device sits on silicon dioxide.

phosphorus via a spin-on dopant. A 20 nm layer of Al_2O_3 is deposited via ALD. We perform electron beamlithography using Microchem PMMA A2 950 with an additional anti-charging layer (Mitsubishi Rayon Aquasave 53za). Following development, we sequentially deposit 5 nm of Al_2O_3, 30 nm of chromium, and finally 40 nm of Al_2O_3 all using electron beam evaporation and perform liftoff of this layered stack. Using the top layer of Al_2O_3 as a hardmask, we etch through the ALD Al_2O_3 layer using a Cl_2, CH_4, H_2 plasma etch. We then etch through the silicon device layer using a mixed-mode Bosch etch. This process aligns the chromium gate layer with the silicon layer without a second lithography step. Finally, we use successive photolithography steps followed by wet chemical etching to create vias through the mask to electrically contact the chromium gate layer on either side of the emitter-collector gap and to the silicon device layers serving as the emitter and collector. Etching through the ALD Al_2O_3 layer requires a thicker hardmask and reduces the minimum achievable emitter to collector gap to approximately 60 nm.

The current-voltage characterization of the field-emission triode is shown in Fig. 3(a). The chromium layer over the blunt collector is referred to as gate 1. As the voltage on gate 1 is decreased, the electric field at the emitter tip is reduced in turn, reducing the Fowler-Nordheim current. The emitter emits electrons into both the collector and the gate, with a ratio of approximately 1.75:1. The second gate over the emitter is partially etched during fabrication, and so, it is ineffective at gating field emission. It is expected that the emitter-side gate could serve as a suppressor for field emission current by depleting the doped silicon emitter of free charges. Increasing the thickness of the ALD Al_2O_3 layer could further reduce gate leakage by reducing the possibility of pin-holes and reducing the likelihood that emitted electrons would travel to the gate rather than the emitter.

In Fig. 3(b), we show a plot of the currents in Fowler-Nordheim coordinates, for currents greater than 50 nA. The y-intercept of each Fowler-Nordheim line increases in magnitude with gate voltage. This corresponds to either an increasing emission area at high gate voltages or a decrease in work



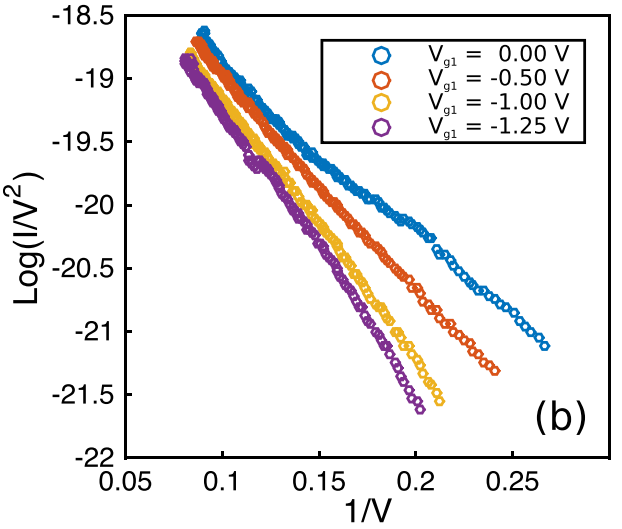


FIG. 3. (a) The current-voltage characteristic for the three-terminal field emission device. The red portion represents the emitter current, the blue portion represents the collector current, and the green portion represents the gate leakage current. (b) The three-terminal Fowler-Nordheim characteristic, plotted for currents greater than 50 nA, confirms that the gate modifies the field emission.

function or both.[21] The slope of the Fowler-Nordheim line is dependent on the work function of the emission site. We perform a similar set of 2D COMSOL simulations to obtain estimates of the work function of the emitting material shown in Table I. As gate voltage increases, the absolute value of the slope of the Fowler-Nordheim line increases, corresponding

TABLE I. Calculated work functions for the three-terminal device obtained by combining fitted Fowler-Nordheim slope data with simulated estimates of the field enhancement factor.

Device	Fitted FN slope (V)	Simulated $k = E/V$	Calculated ϕ (eV)
Three terminal, Vg = 0 V	−13.321	3.22×10^7 1/m	6.33
Three terminal, Vg= −0.25 V	−18.262	3.22×10^7 1/m	5.13
Three terminal, Vg= −0.5 V	−17.040	3.22×10^7 1/m	5.37
Three terminal, Vg= −0.75 V	−18.541	3.22×10^7 1/m	4.902
Three terminal, Vg = −1 V	−20.347	3.22×10^7 1/m	4.77
Three terminal, Vg= −1.25V	−21.74	3.22×10^7 1/m	4.57

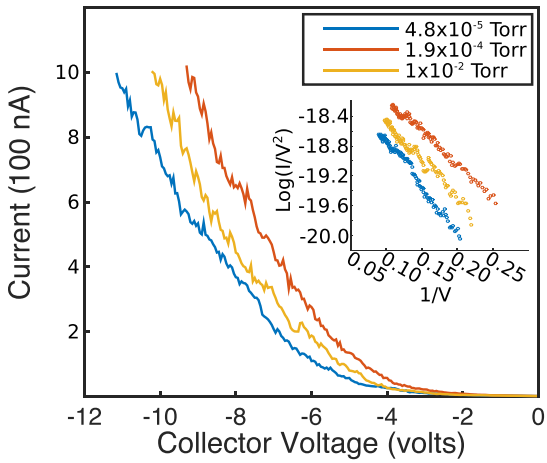


FIG. 4. The current-voltage characteristic of a three-terminal field-emitting device with fixed gate voltages plotted at different pressures of argon gas.

to a decrease in the calculated work function of the emitter towards a limiting value of ~4.5 eV. The limiting value is close to the bulk work function of silicon,[16] and the change is consistent with the change in the intercept of the Fowler-Nordheim plot seen previously. A possible hypothesis is that as the gate voltage increases, the higher field at the emitter tip increases the area of emission to include more of the surrounding silicon around a local hotspot. This would cause the average work function of the emitting area to approach that of silicon.

The operation of field emitting devices at different pressures is an important metric for future packaging and practical use. In Fig. 4, we plot the current-voltage characteristics of a three-terminal field-emitting device with fixed gate voltages at different pressures. We determine the pressure dependence by backfilling our testing chamber with 99.99% pure argon gas and controlling the chip temperature via a heater and thermocouple to 110 °C ± 10 °C. The device was stabilized at each pressure for 5–10 min before the measurement was taken. As expected, even if the pressure is increased by several orders of magnitude, there is no systematic change in the current voltage characteristic greater than the change expected of a single emitter in the same amount of time, as indicated by our earlier time series measurements.

In this work, we have demonstrated practical field emission devices that operate below 10 V and that are CMOS compatible. Our devices represent a promising start toward matching the performance of existing solid-state devices and integrated circuits in terms of current and turn-on voltages. Current CMOS devices operate in the sub 5-V regime and switch milliamps of current. By choosing low work function materials, such as tungsten or very highly doped silicon,[17] and by using thicker emitting layers that can sustain higher current, it is possible that nanoscale field emitting devices can achieve these operating conditions. If nanoscale field emission devices can be practically integrated into circuits, their fundamental characteristics will enable high switching speed, high temperature robustness, and operation in high radiation environments.

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